

## REMARKS

Claims 1-42 are pending. Claims 1-14 and 18-37 have been withdrawn. Reconsideration of all rejected claims is requested in light of the arguments below.

### *Allowable Subject Matter*

Applicant thanks the Examiner for indicating that claims 40-42 contain allowable subject matter

### *Information Disclosure Statement*

References submitted in a Supplemental Information Disclosure Statement dated April 24, 2006, which is available in PAIR, remain unacknowledged.

Reference numbers 4 and 5 of the Supplemental Information Disclosure Statement filed February 1, 2006, which is available in PAIR, were overlooked and not initialed.

A Supplemental Information Disclosure Statement is being filed herewith.

It is respectfully requested that these Supplemental Information Disclosure Statements be considered and that all outstanding PTO Forms 1449 be initialed and returned with the next Action.

### *Claim Rejections Under 35 U.S.C. §112*

Claim 17 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite because of insufficient antecedent basis for the term "the first array." The word "first" is deleted and "the array" is submitted to have sufficient antecedent basis. Therefore, the rejection is believed to be overcome.

### *Claim Rejections Under 35 U.S.C. §102*

Claims 15-17, 38 and 39 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,032,065 to Gonzalez et al. ("Gonzalez").

Claim 15 recites, "the system configured to select a number of planes according to characteristics of data to be stored." No such selection appears to be shown by Gonzalez. In particular, the cited portion of Gonzalez (column 11, lines 47-62) discusses an exemplary memory architecture in which the memory is divided into planes that contain two units. "The memory array is divided into an even number of units, such as eight, two such units 0 and 1 being illustrated in FIG. 12. A pair of adjacent units, termed a plane, may share peripheral

circuits, such as word line decoders." Column 11, lines 27-31. The cited text discusses programming of pages within units 0 and 1 of FIG. 12, which appear to form a plane in this architecture. However, no selection of a number of planes (or units) is disclosed. The cited text does not appear to have any selection of planes according to characteristics of data to be stored (or according to any other criteria). It is unclear what feature of Gonzalez is considered to correspond to the characteristic of the data of claim 15. Clarification is requested.

Claim 15 as amended further recites, "the system configured to program individual erase blocks within each of the selected planes in parallel." Support for this amendment is found throughout the specification, in particular in FIGs. 9A, 9B and paragraphs 0064-0068. No such programming of erase blocks within each of a selected number of planes appears to be shown by the cited text. The cited text discusses programming of blocks of units 0 and 1 of FIG. 12, but does not disclose parallel programming of any other blocks in other planes. Thus, these elements of claim 15 are not disclosed in the cited portion of Gonzalez, and claim 15 is therefore submitted to be allowable.

Claims 16-17 depend from claim 15 and are therefore submitted to be allowable at least for depending from an allowable base claim. In addition, claims 16-17 recite further claim elements that are not disclosed in the reference.

For example, claim 16 recites, "an individual plane is selected according to the number of available erase blocks remaining in the individual plane." No such selection is shown by the cited portion of Gonzalez (column 11, lines 35-44). The cited text is directed to the example of FIG 12, which involves two units (0 and 1). No selection process appears to be disclosed and the number of erase blocks remaining in units 0 and 1 is not disclosed either. Thus, these claim elements are not disclosed and claim 16 is additionally allowable.

Claim 38 recites, "selecting a second number of erase blocks for storage of the first number of sectors, each of the second number of erase blocks located in a different plane," (emphasis added). In contrast, the cited portion of Gonzalez (column 11, lines 27-62) appears to disclose erase blocks located in the same plane. "A pair of adjacent units, termed a plane, may share peripheral circuits, such as word line decoders. Each unit contains a large number of blocks of memory, such as a block 161 in the unit 0 and a block 163 in the unit 1." Column 11, line 30-33. Thus, it seems that blocks 161 and 163 are in the same plane in this architecture, and it is not seen how blocks 161 and 163 correspond to the blocks of claim 38, which are in different planes.

Claim 38 further recites, "the second number being the smallest number of erase blocks that can contain the first number of sectors," (emphasis added). In contrast, the number of erase blocks used in Gonzalez (two blocks, 161 and 163) does not appear to be the smallest number of erase blocks that could contain data 165 and 167. In particular, data 165 and 167 are disclosed as halves of a page, which could alternatively be stored together in the same page in a single block. "Rather than forming a full page from memory cells of a single block, which is usually done, the example shown puts one-half 165 of a given page in the block 161 of the unit 0 and the other one-half 167 of the same page in a block of the unit 1." Column 11, lines 35-39 (emphasis added). Thus, the smallest number of erase blocks that can contain data 165 and 167 would appear to be one block. However, data 165 and 167 are shown stored in two blocks (161 and 163), which is not the smallest number of blocks that could contain them. Therefore, because these features of claim 38 are not disclosed by the cited portion of the reference, anticipation has not been shown.

Claims 39-40 depend from claim 38 and are submitted to be allowable at least for depending from an allowable base claim. In addition, claim 39 recites, "ones of the first number of sectors are stored in an individual one of the second number of erase blocks in a non-sequential order." The Office Action indicated that these features were shown by data, which once split is no longer sequentially stored (apparently referring to data 165 and 167 of FIG. 13). However, because such data is split, it would appear to be partial sectors, not whole sectors. "Sectors of user data smaller or larger than the capacity of the pages are stored across adjacent pages within the individual blocks, except that one-half of each user data sector is stored in one-half of the page in one unit's block and the other one-half of the sector is stored in the remaining one-half of the page in the other unit's block." Column 11, lines 49-54. Thus, there is no storing of "ones of the first number of sectors" in a block, only storage of half sectors in this example. Therefore, claim 39 is additionally allowable.

**Conclusion**

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned at 415-591-1583 would be appreciated.

Respectfully submitted,

9/26/07  
Date

Peter A. Gallagher  
Peter A. Gallagher, Reg. No. 47,584  
on behalf of Allan A. Fanucci, Reg. No. 30,256

**WINSTON & STRAWN LLP**  
**Customer No. 69735**  
**(415) 591-1583**